Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 – 24 (Canceled)

Claim 25 (Original): A column address counter for counting up a column address comprising:

a timing change circuit to switch a timing for counting up the column address in response to a mode switch signal which indicates a first transfer mode or a second transfer mode, wherein data is transferred in synchronization with both of rising and falling edges of a clock signal in the first transfer mode, and the data is transferred in synchronization with only one of the rising and falling edges in the second transfer mode.

Claim 26 (Currently Amended): A column address counter as set forth in claim 25, further comprising:

a clock generating circuit supplying a first and second internal address generating clock**[[s]]** signals;

a first address generating section generating a first internal address in the synchronization with the first internal address generating clock signals;

a second address generating section generating a second internal address in synchronization with the second address generating clock signals.

Claim 27 (Currently Amended): A column address counter as forth in claim 26, wherein the clock generating circuit comprises a clock generator and a frequency divider, the clock generator generating an internal clock signal in response to an external clock signal, the frequency divider receiving the internal clock signal and generating a divided clock signal, and wherein the clock generating circuit outputs the internal clock signal as the first internal address generating clock signal in the first transfer mode and outputs the divided clock signal as the first internal address generating clock signal and the internal clock signal as the second internal address generating clock signal in the second transfer mode.

Claims 28 – 40 (Canceled)

Claim 41 (New): A semiconductor memory device receiving a data strobe signal and receiving an input data at a double data rate, comprising:

a first data latch circuit receiving an internal data strobe signal for latching the input data;

a second data latch circuit receiving the internal data strobe signal for latching the input data;

a first input data latch receiving a data latch signal for latching data stored in the first or second data latch circuit;

a second input data latch receiving the data latch signal for latching data stored in the second or first data latch circuit;

a first write amplifier receiving a control signal for amplifying and transmitting data from the first input data latch to a memory cell array; and

a second write amplifier receiving the control signal for amplifying and transmitting data from the second input data latch to the memory cell array;

wherein in a test mode, said first and second data latch circuits latch the input data, the first and second write amplifier receive data from the first and second data latch circuits via the first and second input data latches respectively, and one of the first and second write amplifier transmits data to the memory cell array in response to the control signal.

Claim 42 (New): The semiconductor memory device as set forth in claim 41, wherein during the test operation mode, the data latch signal is a constant logic level so that the first and second input data latches receives data from the first and second data latch circuits.

Claim 43 (New): The semiconductor memory device as set forth in claim 41, wherein in a read mode of the double data rate, said first data latch circuit latches the input data in response to a rising edge of the data strobe signal, the second data latch circuit latches the input data in response to a falling edge of the data strobe signal and the first and second input data latches store data from the first and second data latch circuits in response to the data latch signal.

Claim 44 (New): The semiconductor memory device as set forth in claim 43, wherein in the read mode, the first and second write amplifiers amplify and transmit data from the first and second input data latches to the memory cell array in response to the control signal.